MSP/34/39

SET A

M.Sc. PHYSICS
SECOND SEMESTER
ELECTRONICS
MSP – 203
[USE OMR FOR OBJECTIVE PART]

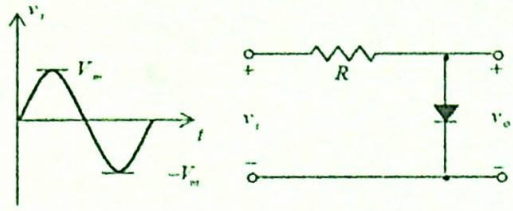
Duration: 1:30 hrs. **Full Marks: 35**

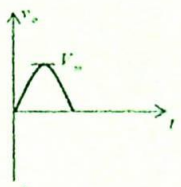
Objective

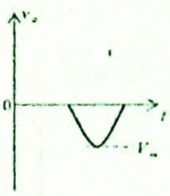
Time: 15 mins. **Marks: 10**

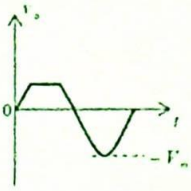
Choose the correct answer from the following: ***1×10=10***

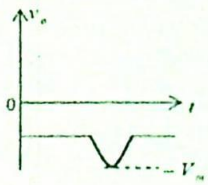
1. Identify the correct output waveform of the circuit shown below (assume the diode to be ideal)



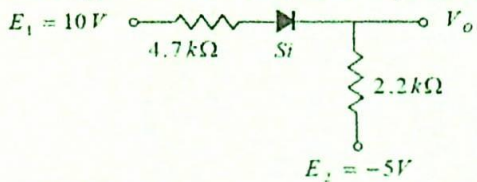
a.


b.


c.


d.


2. The magnitude of the output voltage for the circuit given below is _____Volts.



a. 0.35 b. 0.55
c. 0.45 d. 0.65

3. A Zener diode when biased correctly
   a. Never overheats
   b. Acts as a fixed resistance
   c. Has a constant voltage across it
   d. Has a constant current across it

4. When the differential amplifier is operated single-ended, _____
   a. the output is grounded
   b. one input is grounded and signal is applied to other
   c. both inputs are connected together
   d. the output is not inverted

5. A certain inverting amplifier has R_i of 1 kΩ and R_f of 100 kΩ. The closed-loop voltage gain is_____
   a. 100,000
   b. 1000
   c. 100
   d. 101

6. In a comparator, if we get input as A>B then the output will be _____
   a. 1
   b. 0
   c. A
   d. B

7. Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?
   a. Data Selector
   b. Data distributor
   c. Both data selector and data distributor
   d. DeMultiplexer

8. The truth table for an S-R flip-flop has how many VALID entries?
   a. 1
   b. 2
   c. 3
   d. 4

9. What is one disadvantage of an S-R flip-flop?
   a. It has no Enable input
   b. It has a RACE condition
   c. It has no clock input
   d. Invalid State

10. A J-K flip-flop can be obtained from the clocked S-R flip-flop by augmenting _____
   a. Two AND gates
   b. Two NAND gates
   c. Two NOT gates
   d. Two OR gates

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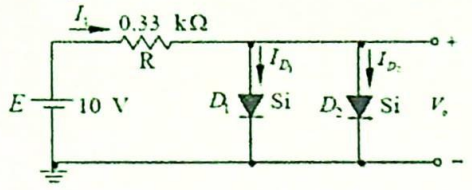
Descriptive

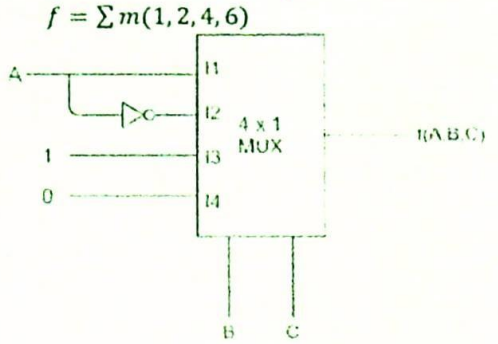
Time : 1 hr. 15 mins. **Marks: 25**

[Answer question no.1 & any two (2) from the rest]

1. Determine V_o, I_1, I_{D1} and I_{D2} for the parallel diode configuration shown in figure below. **5**



2. a. Show that the output function of the circuit shown below is $f = \sum m(1,2,4,6)$ **5+5=10**



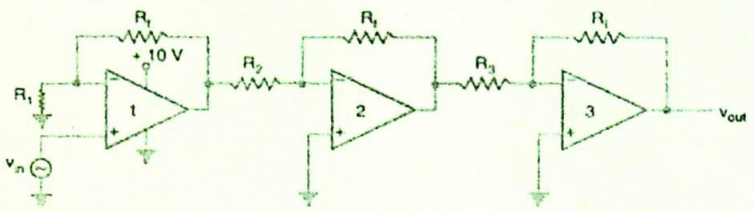
b. Implement $F(A,B,C,D) = \sum m(1,3,4,11,12,13,14,15)$ using 8×1 MUX.

3. a. What do you understand by transistor biasing? What is its need? **2+8=10**

b. Describe the potential divider method of transistor biasing in detail. How stabilization of operating point is achieved by this method?

4. a. Discuss the operation of Op-Amp as integrator and differentiator. 6+4=10

b. A three-stage Op-Amp circuit shown below is used to provide voltage gains of +10, -18 and -27. Find the values of R_1, R_2, R_3 and V_{out}. Use a 270 kΩ feedback resistor for all the stages and input voltage of 150 μV.



5. a. Draw the logic diagram and explain the operation of a Clocked JK Flip Flop for all possible combination of J and K. 4+4+2 =10

b. Draw the truth table, characteristics table, excitation table and state transition diagram for JK Flip Flop.

c. What is race around condition in JK flip-flop? Write the methods to avoid such condition.

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