REV-01
BCA/57/62

2022/08

BACHELOR OF COMPUTER APPLICATION
SECOND SEMESTER
COMPUTER ORGANIZATION & ARCHITECTURE
BCA – 202

(Use Separate Answer Scripts for Objective & Descriptive)

Duration : 3 hrs. **Full Marks : 70**

(PART-A: Objective)

Time : 20 min. **Marks : 20**

Choose the correct answer from the following: ***1X20=20***

1. Number of address bus configured in 8086 microprocessor is_____
   a. 8 b. 10
   c. 32 d. 16

2. Hit ratio is a term used to measure_____ of memory
   a. Performance b. Capacity
   c. Speed d. Hits

3. The VLIW architecture follows _____ approach to achieve parallelism.
   a. SISD b. MIMD
   c. MISD d. SIMD

4. Number of instructions generally available in RISC architecture is _____
   a. 50 b. 100
   c. 150 d. 200

5. _____ are the different type/s of generating control signals.
   a. Hardwired b. Micro-instruction
   c. Micro-programmed d. Both Micro-programmed and Hardwired

6. Which of the following is the correct full form of CISC?
   a. Complex Instruction Sequential Compilation b. Complete Instruction Sequential Compilation
   c. Computer Integrated Sequential Compiler d. Complex Instruction Set Computer

7. The difference in the address and data connection between DRAM's and SDRAM's is _____
   a. The requirement of more address lines in SDRAM's b. The usage of a buffer in SDRAM's
   c. The usage of more number of pins in SDRAM's d. None of the mentioned

8. The controller multiplexes the addresses after getting the _____ signal.
   a. INTR b. ACK
   c. RESET d. Request

9. The drawback of building a large memory with DRAM is _____
   a. The Slow speed of operation
   b. The large cost factor
   c. The inefficient memory organisation
   d. All of the mentioned

10. The bit used to signify that the cache location is updated is _____
   a. Flag bit
   b. Reference bit
   c. Update bit
   d. Dirty bit

11. The number successful accesses to memory stated as a fraction is called as _____
   a. Access rate
   b. Success rate
   c. Hit rate
   d. Miss rate

12. A source program is usually in _____
   a. Assembly language
   b. Machine level language
   c. High-level language
   d. Natural language

13. The ALU makes use of _____ to store the intermediate results.
   a. Accumulators
   b. Registers
   c. Heap
   d. Stack

14. The I/O interface required to connect the I/O device to the bus consists of _____
   a. Address decoder and registers
   b. Control circuits
   c. Address decoder, registers and Control circuits
   d. Only Control circuits

15. The time delay between two successive initiations of memory operation _____
   a. Memory access time
   b. Memory search time
   c. Memory cycle time
   d. Instruction delay

16. The decoded instruction is stored in _____
   a. IR
   b. PC
   c. Registers
   d. MDR

17. Which of the following Signal interrupt has highest priority?
   a. TRAP
   b. NMI
   c. INTR 7.5
   d. INTR 6.5

18. To extend the connectivity of the processor bus we use _____
   a. PCI bus
   b. SCSI bus
   c. Controllers
   d. Multiple bus

19. Number of pins available in microprocessor 8085 is
   a. 56 pins
   b. 40 pins
   c. 20 pins
   d. 32 pins

20. A data transfer technique used by DMA such that the controller transfer one data word at time is called_____.
   a. Cycle stealing
   b. Serial transfer
   c. Burst transfer
   d. Sequence transfer

-- --- --

PART-B : Descriptive

Time : 2 hrs. 40 min. **Marks : 50**

[Answer question no.1 & any four (4) from the rest]

1. Explain the three data transfer modes available in basic computer. **10**

2. a. Define the term superscalar processor. What are the limitations of superscalar processor? **5+5=10**
   b. Draw the block diagram of flag register of a basic computer.

3. a. With a suitable diagram explain the register organization of a basic computer. **5+5=10**
   b. Elaborate the controversy between RISC vs CISC.

4. a. Design a full adder circuit. **5+5=10**
   b. Draw the flowchart of integer multiplication technique in computer

5. Explain the roles of operating system in computer. Why secondary memory is used in computer? **5+5=10**

6. a. What do you understand by 'PSW'? Give the organization of PSW. **5+5=10**
   b. Define, SEL A, SEL B, SEL D, OPR in control unit design.

7. a. What is microinstruction? Explain the process sequence of microinstruction execution. **5+5=10**
   b. Explain the term Parallel processing? Define pipeline.

8. Write short notes on **5+5=10**
   a. IOP
   b. DMA

= = *** = =